

# Altitude SEE Test European Platform (ASTEP): Project Overview, First Results in CMOS 130nm and Perspectives

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**Abstract**— The “Altitude SEE Test European Platform” (ASTEP) is dedicated to real-time soft-error rate (SER) testing of semiconductor memories. The platform, located in the French Alps on the “Plateau de Bure” at 2552m, has been operational since March 2006. This test facility includes a proprietary automatic test equipment specially designed for static memory (SRAM) testing and secured remote control operation via internet. First real-life SER measurements on 3.6 Gbit of SRAMs manufactured in CMOS 130 nm technology are reported, as well as the comparison between real-life and accelerated SER. Project perspectives for CMOS 65nm SRAMs are finally reported.

**Index Terms**— Single-Event Effects (SEE), Single-Event Rate (SER), real-life testing, atmospheric neutrons, terrestrial radiation environment, static memory, accelerated tests, SER simulation, alpha-SER, neutron-SER.

## I. INTRODUCTION AND PROJECT MILESTONES

SINCE terrestrial cosmic-rays have been identified to be at the origin of soft errors in modern integrated circuits, the estimation of soft error rates (SER) is rapidly becoming a major consideration for reliability aspects at device, circuit and system levels [1]. For deep submicron technologies, SER of chips is becoming a vital customer issue and its determination is still an open challenge, not only to investigate and understand technology sensitivity but also to extrapolate the trends for future generations of circuits.

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Table I. Location and main environment characteristics of the ASTEP Platform (After Ref. [2]).

ASTEP, Plateau de Bure, France		
Latitude (°N)		44.6
Longitude (°E)		5.9
Elevation (m)		2550
Atm. depth (g/cm <sup>2</sup> )		757
Cutoff rigidity $\gamma$ (Gy)		5.0
Relative	Active Sun low	5.76
	Quiet Sun peak	6.66
	Average	6.21



Figure 1. General view of the Observatory on the Plateau de Bure. The ASTEP platform is hosted in Building POM2 indicated in the figure (Photo courtesy of IRAM).

Different experimental and simulation approaches are known to estimate SER: accelerated testing using alpha, neutron or proton source/beam, life testing under natural environments, modeling and software simulation at device or circuit level, combination of experimental/simulation approaches [1-2]. In contrast with accelerated testing which is relatively easy to conduct, cheaper and fast (a few hours/days is generally sufficient to obtain confident results), life testing is clearly time consuming and expensive. But it appears as the unique experimental solution to accurately estimate SER, ensuring that the test does not introduce artificial results due, for example, to beam uniformity/fluctuations, dosimetry errors, chip disorientation or difference in spectrum (largely introduced by the cut-off energy of the accelerator which is always well below cosmic ray energies). Life testing can also address SER at system level for complex electronic solutions and, installed in an underground site, provide an efficient method of monitoring for radioactive contamination. On the

contrary, when based at altitude to increase the flux of particles (primarily neutrons, but also pions and protons), SER by life testing can be accelerated by a factor  $\sim 2-15$  depending on the earth location of the test site.

The project of an “Altitude SEE Test European Platform”, located in the French Alps and simultaneously opened to industrials and laboratories to conduct, in the same place, qualification tests or research works, was initiated by STMicroelectronics and JB R&D in 2001. The ASTEP consortium was created in 2003 and operated by the CNRS and L2MP laboratory in 2004, in the framework of a multi-partner European-national funding program (the preliminary project was presented during the RADECS’05 industrial exhibition at the booth L2MP-CNRS). At the end of 2004, Bertin Technology (Aix-en-Provence, France) was selected as the industrial integrator of the automatic tester equipment. The construction of the machine was conducted in 2005, including one trimester of tests and qualifications and the preparation of the test area on the Plateau de Bure. Finally, the equipment was installed in altitude, on the Plateau de Bure, in February/March 2006 and the first campaign of SER life testing officially began on March 2006. The aim of this paper is precisely to present a brief overview of this project and to report the first experimental results obtained during this initial 5-month operation period.

## II. TEST PLATFORM AND EXPERIMENTAL DETAILS

### A. Location and environment

The ASTEP platform is located in the French Alps at 2,552m of elevation. The installation is hosted by the Institute for Radio-astronomy at Millimeter Wavelengths (IRAM) on the Plateau de Bure in the Dévoluy Mountains. Fig. 1 shows a general aerial view of the observatory on the Plateau: the ASTEP platform is installed in an ancient radio-telescope building reconverted into an altitude laboratory platform (one floor standard concrete slab building). The main environment characteristics of the ASTEP platform are summarized in Table I. Since 2006, this test location has been referenced in the latest release of JEDEC Standard JESD89A [3]. Data of Table I corresponds to values of Table A3.B in Ref. [3].

### B. The Automatic Test Equipment (ATE)

The ASTEP masterpiece is a specially designed and universal SRAM automatic test equipment (ATE), capable of monitoring several thousands of synchronous/asynchronous SRAM memories and performing all requested operations such as writing/reading data to the chips, comparing the output data to the written data and recording details on the different detected errors. The ATE hardware and software have been designed and developed by BERTIN Technologies (Aix-en-Provence, France), in collaboration with L2MP-CNRS and STMicroelectronics. The design of both the hardware and software components of the system follows all the specifications of the JEDEC SER test standard [3]. Fig. 2 shows a schematic representation of the whole test equipment. This system is divided in two identical subsystems,

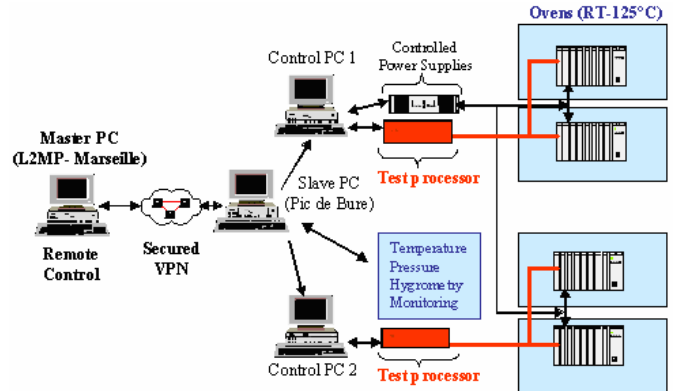


Figure 2. Schematic description of the automatic test equipment (ATE) designed and built to perform real-time SER tests on static memories. The ATE is divided in two networked subsystems (Astep1 and Astep2), capable of monitoring two memory racks (640 test chip per rack) placed in temperature-controlled ovens.

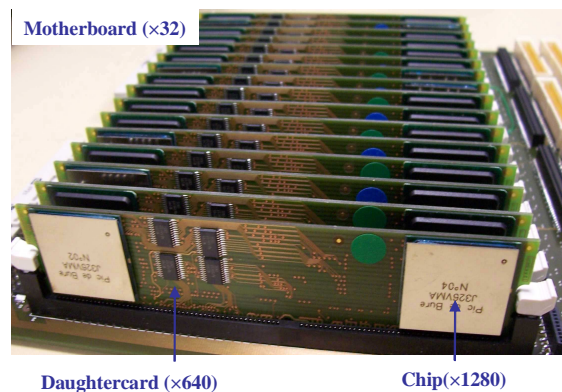


Figure 3. Detail of one motherboard containing 40 daughtercards and 80 test chips (2 per daughtercard). The complete ATE system is designed to test a maximum of 1280 chips dispatched on 32 motherboards and 640 daughtercards.

Astep1 and Astep2, capable of independently performing an automatic survey of two racks of memories placed into temperature-controlled ovens (RT-125°C). Each rack contains 8 motherboards; each motherboard connects 40 daughtercards and each daughtercard drives 2 test chips. The daughterboards (and consequently the chips) are oriented face horizontally. The current consumption of each daughtercard, i.e. of each pair of devices, is real-time monitored on 4 supply lines on a total of 5 for Single Event Latchup (SEL) detection. This explains the relative complexity of the electronic circuitry developed at the level of each daughtercard (current monitoring) and for each motherboard (the system is able to disconnect a given daughtercard in case of abnormal power consumption; the current intensity threshold is directly controlled by the software interface as an input parameter of the test). Fig. 3 shows a zoom of a motherboard with its daughtercards and test chips. The maximum capacity of the ATE in the current configuration is 1280 test chips. Of course, the system is modular and it will be able to received additional racks for future experiments. The ATE can be completely controlled in remote control mode via a virtual private network (VPN) on internet. This allows the users to perform all control operations during a real-time experiment and to access all the data in real-time.

### C. Test procedure

The test procedure implemented in the ATE control software allows the discrimination of the following error types as a function write/read and rewrite/reread operation results: "Transient Soft Error" (TSE), sometimes called dynamic read error; "Static Soft Error" (SSE), i.e. classical bit flip; "Single-Event Hard Error" (SHE), sometimes referred as stuck bit.

When an error is detected, the software increments the data-log file with all information concerning the fail: date and time, type of error (TSE, SSE or SHE), written pattern and read pattern, round number (i.e. scan number of all memories from the beginning of the experiment), testchip identification (rack, board, slot and chip numbers) and logical address. An additional software is used to perform a physical mapping of the bit flips. This mapping is used to discriminate logical multi-bit upsets (MBU) from physical multi-cell upsets (MCU), as recently recommended by [3].

### D. Devices under test

The first real-time testing campaign has been currently performed on bulk static memories (SRAM) fabricated by STMicroelectronics using a CMOS 130 nm commercial technology (PBSG-free) process (6-transistor cell with a bit cell area of  $2.50 \mu\text{m}^2$ ). This technology was extensively characterized in previous works using alpha irradiations (with both ST and L2MP setups) and neutron accelerated SER tests performed with two continuous neutron sources available in North-America (TRIUMF and LANSCE facilities). The use of a mature and well-characterized technology is important for the validation of ATE functionalities and data comparison between accelerated and life time testing. The test chip is composed of different memory cuts; only a single cut of 4 MBit has been used (i.e. connected) for the present measurement campaign. The ATE was initially loaded at 72% of its maximal capacity with 492 test chips in the Astep1 subsystem and 424 chips in Astep2, respectively. This represents a total of 912 chips, i.e. 3,664 MBit under test.

## III. EXPERIMENTAL RESULTS

### A. Real-time testing results

Fig. 4 shows the cumulative fail number versus test hours for the two subsystems Astep1 and Astep2 during the period March 31 – September 6, 2006. These events correspond to Static Soft Errors (SSE) detected under nominal test conditions ( $V_{DD} = 1.2 \text{ V}$ , room temperature and checkerboard pattern for all devices). Because of several maintenance operations in the test room, the two subsystems were subjected to interruptions during this period. However, the number of MBit $\times$ h cumulated during these five months approaches  $10^7$  MBit $\times$ h, which gives an excellent confidence interval on the extrapolated SER, as shown in the following. A total of 44 fails was detected, including 38 single event upsets and 3 MBU. These later involved 2 physical adjacent bit cells in all cases.

From data of Fig. 4, we estimated real-time SER, shown in Fig. 5, using the following expression:

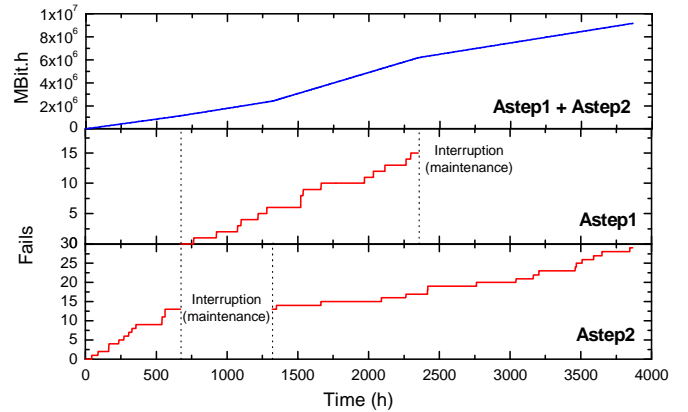


Figure 4. Cumulative fail numbers versus test hours for the two boards Astep1 and Astep2 of the ATE. The experiment started on March 31, 2006 and finished on September 6, 2006 under nominal test conditions ( $V_{DD} = 1.2\text{V}$ , room temperature, checkerboard). The cumulated number of MBit $\times$ h versus test hours is also indicated (approaching  $\sim 10^7$  MBit $\times$ h at the end of the test period).

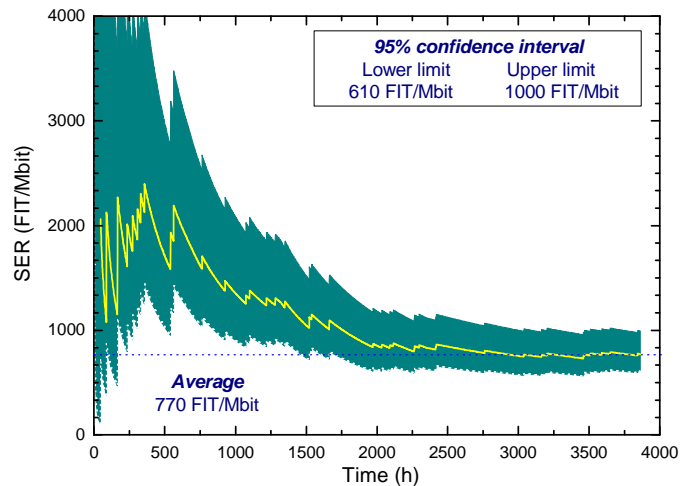


Figure 5. Estimated real-time SER (FIT/Mbit) versus test hours calculated from data of Fig. 7. 95% confidence intervals are also indicated. The average acceleration factor value of 6.21, given in Ref. [1], was used to estimate this real-time SER. The erratic character and high value of the SER in the first  $\sim 1000$  hours are due to the very low number of cumulated fails during this period, introducing a large error in the evaluation of the ratio  $N_r/\Sigma_r$  in Eq. (1).

$$\text{SER} = \frac{N_r}{\text{AF} \times \Sigma_r} \times 10^9 \text{ (FIT/MBit)} \quad (1)$$

where  $N_r$  is the number of errors observed at time  $T_r$ , AF is the acceleration factor of the test location and  $\Sigma_r$  is the number of MBit $\times$ h cumulated at time  $T_r$ . The acceleration factor value is considered equal to  $\text{AF}=6.21$  for the ASTEP platform. It corresponds to the estimated relative neutron flux (average value) of the Plateau de Bure with respect to the reference flux of New-York City, as reported in Table A.3-B of Ref. [3]. 95% confidence interval upper and lower limits [3] are also indicated in Fig. 5. An average value of 770 FIT/Mbit is obtained, with lower and upper confidence limits equal to 610 and 1000 FIT/Mbit, respectively. In addition, Fig. 5 shows that the convergence of SER vs. test hours is reached in approximately 2000-2500 h, i.e. for  $4\text{-}6 \times 10^6$  MBit $\times$ h. Beyond this duration, the SER remains constant around 770 FIT/Mbit.

### B. Accelerated versus real-time SER

In complement to real-time characterization, both neutrons and alpha irradiations (under nominal test conditions) were performed on several test chips issued from the same technological lot. Neutron experiments were performed using the continuous spectrum sources available at both the Los Alamos Neutron Science Center (LANSCE) and at the Tri-University Meson Facility at Vancouver, (TRIUMF). Additional alpha-irradiation measurements were also performed using two different Am<sup>241</sup> sources at ST and at L2MP laboratory. SER values obtained with these two setups agreed within  $\pm 10\%$ . Fig. 6 shows the normalized accelerated results for this commercial CMOS 130nm SRAM. Average values of 380 FIT/Mbit and 665 FIT/Mbit have been obtained for alpha-SER and neutron-SER, respectively.

If we try now to compare, as in [4], these accelerated and real-time test results, one has to remind that the SER given by the altitude experiment (i.e. 770 FIT/Mbit) must be corrected from the impact of alpha contamination affecting all tested devices. In other words, this signifies that a certain number of fails detected by the ATE during the test period have been induced by alpha particles and not by neutron interactions. Supposing a real-time alpha-SER equal to the value given by accelerated tests (i.e. 380 FIT/Mbit) and taking into account the acceleration factor (AF=6.21) of the test location only for neutron-induced fails, we obtain a corrected neutron failure-in-time of 710 FIT/Mbit. This corrected value is very close to the accelerated neutron-SER value equal to 665 FIT/Mbit, demonstrating, in this case, a very good agreement between the two estimation methods within the experimental error margins.

### C. Simulated versus real-life SER

Three Dimensional (3D) Monte-Carlo simulations used to predict neutron-SER were also performed for this SRAM circuit, using a proprietary radiation simulator developed by STMicroelectronics [5-6]. This simulation code considers the exact layout of the memory cell and calibrated TCAD results as inputs. Simulation results for nominal conditions ( $V_{DD} = 1.2$  V, room temperature) give a typical neutron failure-in-time of 700 FIT/Mbit. This value is very close to those corresponding to both accelerated and real-time experiments.

## IV. PERSPECTIVES FOR CMOS 130 AND 65 nm

Since September 9, 2006, a new measurement campaign has been started with the same 130 nm SRAM circuits. The objective is now to quantify the impact of several key-parameters, i.e. the power supply voltage, the test temperature (up to 125°C) and the configuration of the written pattern, on the real-time SER. Another objective is also to further compare real-time and accelerated tests for which data is already available on this test vehicle.

Beyond this work currently in progress, STMicroelectronics (Crolles), with its partners NXP (formerly Philips Semiconductor) and Freescale (formerly Motorola), is envisaged to test a new circuit on the ASTEP platform within the following months. This circuit is a CMOS 65nm test vehicle for library qualification and process monitoring. It

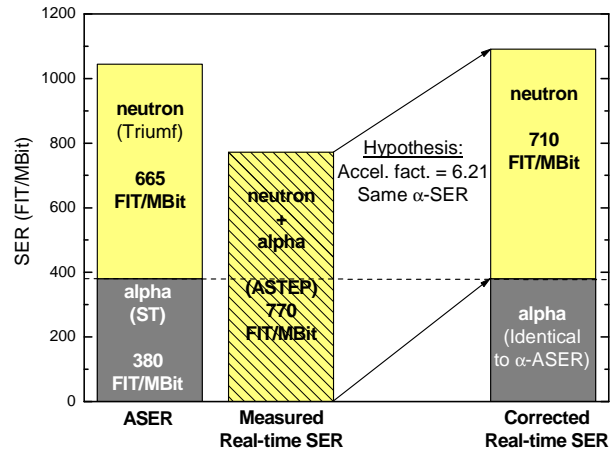


Figure 6. Comparison between the accelerated (ASER) and the real-time SER estimated in Fig. 5. Accelerated tests were performed at Triumf facility for neutron-ASER and at both ST-Crolles and L2MP-Marseille for alpha-ASER characterization, respectively. Real-time SER data of Fig. 5 is corrected from the contribution of alpha disintegrations, considering a same alpha-SER for both accelerated and real-time experiments.

contains 8.5 Mb of single port SRAM (bit cell area of 0.525  $\mu\text{m}^2$ ) already characterized this year from an accelerated-test point-of-view with neutrons at LANSCE and TRIUMF, as well as with alphas at STMicroelectronics. About 1000 test chips, representing a memory capacity up to 8 Gbit, should be mounted in the automatic test equipment by the beginning of 2007.

The last near-term perspective for the ASTEP platform is the development, in 2007, of an *in situ* neutron monitor, installed close to the test equipment (directly in the test room) to try to correlate the observed circuit fails with the total neutron flux incident on the experimental area. This equipment, based on high pressure He<sup>3</sup> neutron proportional counters, should be completed by a high sensitivity neutron spectrometer in 2008-2009 for a more accurate characterization of the ASTEP radiation environment.

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