

# Real-Time Neutron and Alpha Soft-Error Rate Testing of CMOS 130nm SRAM: Altitude *versus* Underground Measurements

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**Abstract**— This work reports real-time soft-error rate (SER) testing of semiconductor static memories in both altitude and underground environments to separate the component of the SER induced by the cosmic rays (i.e. primarily by atmospheric neutrons) from that caused by on-chip radioactive impurities (alpha-particle emitters). Two European dedicated sites were used to perform long-term real-time measurements with the same setup: the Altitude SEE Test European Platform (ASTEP) at the altitude of 2252m and the underground laboratory of Modane (LSM, CEA-CNRS) under 1700 m of rock (4800 meters water equivalent). Experimental data obtained using 3.6 Gbit of SRAMs manufactured in CMOS 130 nm technology are reported and analyzed. Comparison with accelerated and simulated SER is also discussed.

**Index Terms**— Single-Event Rate (SER), real-time testing, atmospheric neutrons, terrestrial radiation environment, static memory, accelerated tests, SER simulation, alpha contamination, neutron-induced SER.

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## I. INTRODUCTION

AS Metal-Oxide-Semiconductor (MOS) devices continue to be scaled down, the sensitivity of integrated circuits to radiation coming from the natural terrestrial environment (primarily atmospheric neutrons) or induced by on-chip radioactive impurities (source of alpha particles) has been found to seriously increase and at least sufficiently to be considered as a major reliability problem by several semiconductor manufacturers [1]. Current ultra-scaled memory ICs become more and more sensitive to single-event-upset (SEU) because of the constant reduction of the supply voltage and node capacitance, resulting in a decrease of the so-called “critical charge” used to store logical information [2-3]. However, the sensitivity of a given technology to atmospheric neutrons or alpha emitters (present into the chip) has not necessary the same magnitude and its impact on the soft-error rate (SER) must be carefully evaluated, i.e. separated in terms of fail occurrence or failure-in-time (FIT).

This work precisely deals with the experimental determination of neutron and alpha induced SER from long-term real-time experiments performed in two very different environments: the first one in altitude to strengthen natural neutron irradiation, the second one underground to completely screen this atmospheric contribution and to quantify the remaining alpha SER directly induced by the presence of radioactive impurities of alpha emitters (Pb, U, Th,...) in the chip materials. Tests have been performed using a CMOS 130nm commercial technology; no BPSG was used in the Back-End Of Line (BEOL) of our DUTs, thus eliminating the major source of <sup>10</sup>B in the circuits and drastically reducing their possible interaction with low energy neutrons (in the thermal range and below) [1-3].

The paper briefly describes, in section II, the test environments, equipment and circuits used in this study before detailing and analyzing real-time experimental data in section III. Comparison with accelerated SER is finally presented to accurately evaluate the alpha emissivity of circuit materials.

## II. TEST PLATFORMS AND EXPERIMENTAL DETAILS

Real-time SER tests were successively performed on two dedicated sites with exactly the same setup, including the automatic test equipment, the control software and more than one thousand SRAM memory ICs. Altitude measurements

TABLE I  
LOCATION AND MAIN ENVIRONMENT CHARACTERISTICS OF THE ASTEP  
PLATFORM (AFTER REF. [5]).

ASTEP, Plateau de Bure, France		
Latitude (°N)	44.6	
Longitude (°E)	5.9	
Elevation (m)	2552	
Atm. depth (g/cm <sup>2</sup> )	757	
Cutoff rigidity (GV)	5.0	
Relative neutron flux	Active Sun low	5.76
	Quiet Sun peak	6.66
	Average	6.21

were performed during the period March 31, 2006 – November 26, 2006 on the ASTEP platform at the altitude of 2252m with respect to sea level. Since October 16, 2007, the experiment has been running at the underground laboratory of Modane (LSM) in a low cosmic ray environment to detect and quantify the part of the SER induced by internal (i.e. on-chip) radioactive contamination. In the following, we briefly describe the test environments and give some key details about the test equipment, the SRAMs and the test procedure used.

#### A. The ASTEP platform

ASTEP is a dual academic research and R&D platform founded by STMicroelectronics, JB R&D and L2MP-CNRS in 2004 [4]. The current platform, operated by IM2NP-CNRS (formerly L2MP), is dedicated to real-time SER testing of semiconductor circuits and systems. Located in the French Alps on the desert Plateau de Bure at 2552m, in a low electromagnetic noise environment, the platform is hosted by the Institute for Radio-astronomy at Millimeter Wavelengths (IRAM). The ASTEP platform is installed in an ancient radio-telescope building reconverted into an altitude laboratory platform (one floor standard concrete slab building). ASTEP is fully operational since March 2006 and is referenced in the JEDEC standard JESD89A [5]. In complement to SER testing facilities, ASTEP is now providing in situ real-time neutron monitoring using a super 3-NM64 neutron monitor. Table I gives the main environment characteristics of the ASTEP platform, as reported in Table A3.B of Ref. [5].

#### B. The underground laboratory of Modane (LSM)

The underground laboratory of Modane is located about 1700 m under the top of the Fréjus mountain (4800 meters water equivalent), near the middle of the Fréjus highway tunnel connecting France and Italy [6]. It was created in 1983 in order to conduct particle physics and astrophysics experiments in a strongly reduced cosmic ray background environment. Due to the depth of the LSM, the particle flux inside the laboratory is extremely reduced:

- 4 muons/m<sup>2</sup>/day corresponding to a two million reduction factor compared to the flux at sea level;
- 3x10<sup>3</sup> fast neutrons/m<sup>2</sup>/day (in the energy range 2-6 MeV) emitted by natural radioactivity from the rock, the neutron component of cosmic rays being totally eliminated at this depth. Table II gives measured radioactivity levels of the rock and concrete obtained by gamma spectrometry.

TABLE II  
RADIOACTIVITY LEVELS OF THE LSM CAVITY ROCK AND CONCRETE [6].

	<sup>238</sup> U	<sup>232</sup> Th	<sup>40</sup> K
Rock	(0.84±0.2) ppm	(2.45±0.2) ppm	(0.213±0.03) Bq.g <sup>-1</sup>
Concrete	(1.9±0.2) ppm	(1.4±0.2) ppm	(7.73±1.3)×10 <sup>-2</sup> Bq.g <sup>-1</sup>

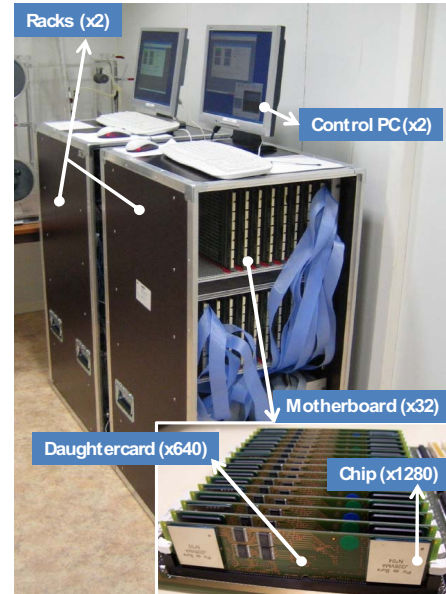


Fig. 1. General view of the SRAM automatic test equipment (here photographed at LSM). Inset: detail of one motherboard containing 40 daughtercards and 80 test chips (2 per daughtercard). The complete system is designed to test a maximum of 1280 chips dispatched on 32 motherboards and 640 daughtercards.

Finally, the Radon in the laboratory is maintained at a very low rate of ~20 Bq/m<sup>3</sup> owing to a air purification system which totally renews the volume of the air inside the laboratory twice an hour.

#### C. Test equipment, circuits and procedure

Fig. 1 shows the SRAM automatic test equipment, specially designed and constructed for the study. This system is capable of monitoring several thousands of synchronous/asynchronous SRAM memories and performing all requested operations such as writing/reading data to the chips, comparing the output data to the written data and recording details on the different detected errors. The complete system has been described in detail in Refs. [4,7]. The different hardware and software components have been designed to strictly follow all the specifications of the JEDEC Standard JESD89A [5]. Particular precautions were taken to minimize digital noise sources and to discriminate memory soft errors from eventual transient errors possibly induced by the system itself. For maximizing the test equipment stability, the control PC and the DUTs should have been ideally split into two different locations. However, Refs. [2,8] with similar system configurations as ours have not reported any test artifact due to its compactness.

Real-time measurements have been currently performed on bulk SRAMs fabricated by STMicroelectronics using a CMOS 130nm commercial technology process, PBSP-free as previously mentioned. This technology was extensively



